REMARKS

Claims 1, 3, 5-12, 14, 15, 17, 18, 20 and 24-31 are pending in the application.

Claims 1, 3, 5-12, 14, 15, 17, 18, 20 and 24-31 are rejected.

Claims 1 and 24-28 are rejected under 35 U.S.C. 103(a).

Claims 3, 5-12, 14, 15, 17, 18, 20 and 29-31 are rejected under 35 U.S.C. 103(a).

The applicant requests reconsideration and allowance of the claims in view of the remarks below.

Claim Rejections – 35 USC § 103

Claims 1 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deering, et al. (US Patent No. 5,544,306). The applicant respectfully traverses the rejection.

Claims 1 and 28 recite, among other limitations, a data modifying circuit adapted to receive corresponding new external depth data of the object from the memory controller; if the external depth data is transferred, then over-write the internal depth data with the transferred external depth data. Claim 12 essentially recites similar limitations: writing from the compare circuit the external depth data over the corresponding internal depth data in the memory cell array.

The Examiner rejects claims 1 and 28 by asserting that Deering describes transferring external depth data from the data modifying circuit 58 to the memory cell array 56, which is connecting line 202, and over-writing the internal depth data with the transferred external depth data 202. The Examiner continues by reciting Deering, column 17, lines 1-10, wherein the pixel buffer write enable signal 276 enables writing of the write port data 202 into the pixel buffer 56.

But it is important to note that write port data 202 is not external depth data that was received from the memory controller 70. In detail, Deering's Compare Unit 235 (FIG. 8) compares old data O[31..0] with new data N[31..0] that is received via line 162 and 64 from the rendering controller 70. But the new data N[31..0] stops at the compare unit 235 and does not get written into the memory cell array 56. Instead, as Deering and the Examiner explain, the write port data 202 is written into the pixel buffer 56. And write port data 202 is a product of only the ROP Blend Units 230-233 and clearly not external depth data that was received from the memory controller 70, as claims 1 and 28 require.

Deering's FIG. 9 shows detail of one of the ROP blend units 230 having an output 202. New external data N[7..0] is received through port 250 in the left of the figure. This data is blended and altered as explained by Deering in column 15, line 62 through column 16, line 37, after which data 202 is output. Thus, write port data 202 is not external depth data from the memory controller as claims 1 and 28 require.

The Examiner rejects claim 12 by combining Deering with Dowdell. But Deering fails to teach limitations of claim 12 as recited above, as explained regarding claims 1 and 28, and Dowdell fails to make up for Deering's shortcomings.

In conclusion, the applicant submits that Deering fails to teach all of the limitations of each of claims 1, 12, and 28 and that one skilled in the art would find no reason to modify Deering to teach or make obvious these limitations. Thus, lacking a *prima facie* showing of obviousness, these claims are allowable over the Examiner's cited references.

For the foregoing reasons, reconsideration and allowance of the claims of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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